InnoLight BE5001

10 Gb/s BERT

Features

Multiple Data Rates at 10G: OC192/10GbE/FEC/WAN
Dual channel electrical and optical Interfaces
PRBS and User Pattern
Small Package
Ultra Low Power Consumption
Low Cost Solution for Production Testing
Controlled by User Software on External PC Connected by USB Interface
Free Labview Driver
InnoLight Technology is an established global technology company that provides test solutions for communications industry. With our unique insight and background within telecom and datacom industry, we deliver low cost, high performance test instruments and automatic test sets for high-speed communications components design and manufacturing. InnoLight BE5001 10G BERT is a high performance, low cost equipment suitable for transceiver and TOSA/ROSA production testing.

**Functional Block Diagram**

[Diagram showing USB, Power Supply, Error Detector, Clock, Pattern Generator, O/E E/O, LOS/LOL, IN+/-, OUT+/-, TRG OUT]
Eye Diagram

* Measured at PRBS $2^7$-1, 10.3125 Gb/s.

System Specification

Data rate
The same data rate applies for pattern generator electrical out and optical out, and for error detector electrical in and optical in.

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<table>
<thead>
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<tbody>
<tr>
<td>OC192</td>
<td>9.95328 Gb/s</td>
</tr>
<tr>
<td>10GBE LAN</td>
<td>10.3125 Gb/s</td>
</tr>
<tr>
<td>OC192 with FEC</td>
<td>10.709225 Gb/s</td>
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<tr>
<td>10GBE LAN with FEC</td>
<td>11.095727 Gb/s</td>
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<tr>
<td>Accuracy</td>
<td>$\pm$ 50 ppm</td>
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<tr>
<td>Any-rate</td>
<td>9.95Gb/s–11.4Gb/s (optional)</td>
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Operating system
The GUI software supplied runs on Windows 2000 or XP by a USB interface.

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### Pattern Generator

- **Pattern**: PRBS7, PRBS31, 64bit user pattern
- **Polarity**: Inverted or non-inverted
- **Electrical interface**: SMA, differential, 100ohm, AC coupled
- **Output swing**: 380mV ~ 770mVpp Typical
- **Jitter (rms)**: 2 ps Typical (20%-80%)
- **Jitter (peak to peak)**: 13 ps Typical (20%-80%)
- **Rise/Fall Time**: 34 ps Typical
- **Optical interface**: Support 850nm, 1310nm, 1550nm
- **External reference clock Input**: 1/64 clock (optional) to support any-rate from 9.95Gb/s-11.4Gb/s
- **Trigger Output**: 1/64 clock

### Error Detector

- **Pattern**: PRBS7, PRBS31, 64 bit user pattern
- **Polarity**: Inverted or non-inverted
- **Electrical interface**: SMA, differential, 100ohm, AC coupled
- **Input sensitivity**: 8mV~1000mVpp
- **Optical interface**: Support 850nm, 1310nm, 1550nm
- **Clocking mode**: Integrated CDR

### General

- **Power Supply**: AC input 220 V ± 10%
  - AC input 85-265 V (optional)
- **Power consumption**: 5W Max
- **Operating temperature**: 0°C to 55°C
Outline

Length: 380mm
Width: 300mm
Height: 80mm

Front Panel

Rear Panel

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Application

10G XFP/SFP+ Test Diagram

10G ROSA Sensitivity Test Diagram
10G TOSA High Speed Performance Test Diagram

<table>
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