pB10A

The convenient small hand held 10 Gb/s CDR, BERT and Clock Synthesis Unit

Features

- Data rates from 9.95 Gb/s to 11.3 Gb/s
- Recovers 10 Gb/s clock and data from incoming serial data stream
- Integrated pattern generator provides PRBS 2^{31}–1, 2^{23}–1, 2^{7}–1, and custom serial output patterns
- Build in PRBS Checker and BER counter/ calculator
- Programmable internal clock synthesizer
- Complies with XFP MSA standards
- Small sized hand held device (105 mm × 144 mm × 33 mm)
- Configuration and management via GUI or API interface to PC, Error logs
- Inexpensive, small and universal 10 Gb/s test gear

Transmitter Features

- Serial data output 9.95 to 11.35 Gb/s (CML)
- Line rate serial transmitter clock output (CML)
- Polarity inverter
- De-emphasis capability

Receiver Features

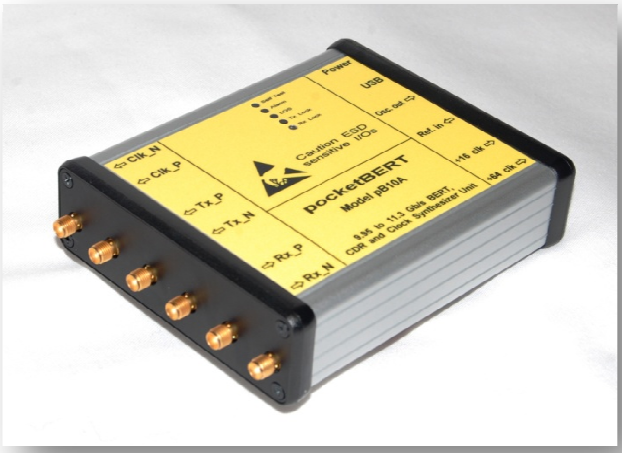
- Single-Ended or Differential inputs
- Continuous 9.95 to 11.35 Gb/s data rates
- 20 mV input sensitivity
- Rx Lock Detect Indicator
- LOS/RSSI
- Polarity inverter
- ISI compensation

Clock Synthesizer Features

- 10 MHz to 760 MHz continuously programmable clock output (CML)

Description

The pB10A is a fully integrated 10 Gb/s clock and data recovery (CDR) unit with serial 10 GHz clock output, PRBS generator/checker and BER calculator unit. The unit recovers SONET STS192 and 10 Gb/s Ethernet/Fiber Channel clock and data streams in the entire data range from 9.95 Gb/s to 11.3 Gb/s. The build-in PRBS generator and checker enable the unit to test the BER of an electrical or optical link.



There is no need for an external reference clock as the unit uses an internal programmable clock generator. If needed an external reference clock can be applied.

CDR mode

The pB10A receives a serial 10 Gb/s data stream from an O/E converter (APD or PIN) or any other electrical source and recovers clock and data. Typical applications are to extract the 10G clock while testing e.g. optical modules or other electrical PHY components where the testing equipment requires a recovered clock.

BERT mode

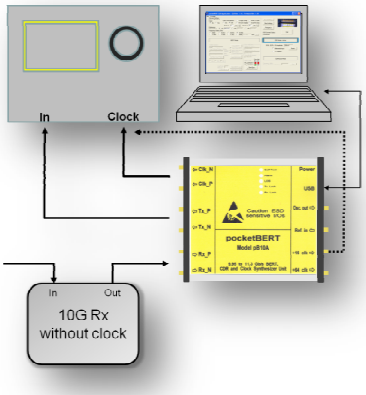
The pB10A has the capability to generate and check various 10 Gb/s PRBS patterns (2^{31}–1, 2^{23}–1, 2^{7}-1 and custom defined). In this mode the unit can be used to evaluate 10 Gb/s components or links with or without XFP, SFP modules. Provides a cost-effective source to generate non synchronized 10 Gb/s traffic e.g. for DWDM test beds.

Programmable Clock Synthesizer mode

The unit can also be used as a standalone precision wide range frequency source. It covers the range from 10 MHz to 760 MHz.

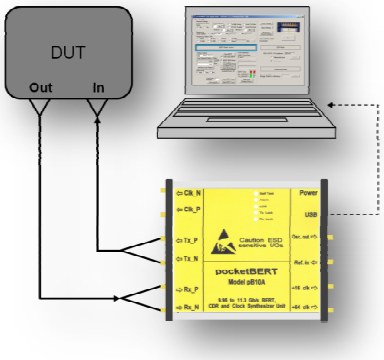
CDR mode

The pB10A receives a serial 10 Gb/s data stream from an O/E converter (APD or PIN) or any other electrical source and recovers clock and data over the 9.95 Gb/s to 11.35 Gb/s frequency range. The recovered clock at line rate as well as divided by 16 and 64 is externally available for further use. If needed an external reference clock can be provided to the CDR. In this case next to the divide by 16 and 64 there is also the possibility to feed a divide by 66 reference frequencies.



BERT mode

The pB10A has the capability to generate and check various 10 Gb/s PRBS patterns: 2^{31}–1, 2^{23}–1, 2^{7}-1, and custom defined. In this mode the unit can be used to evaluate 10 Gb/s components or links with or without XFP, XFP+, SFP+ modules. On the receive path the incoming data stream is recovered and analyzed in the PRBS checker. BER values are read, calculated and displayed in the GUI. Using several units in parallel a cost-effective source can be realized to generate non synchronized 10 Gb/s traffic e.g. for DWDM test beds.



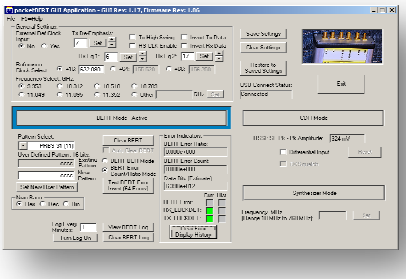
Clock Synthesizer Mode

With all CDR/PRBS features disabled the pB10A unit can be used as a programmable, universal any-rate clock source from 10 Mbps to 760 MHz.

GUI Interface

The Graphical User Interface (GUI) software controls the pB10A. The software runs on a PC/Laptop and uses a USB 2.0 interface to communicate with the pB10A. The software runs on the Windows 2000, XP, Vista and Windows 7 operating systems.
The GUI let's you select one of three modes:

- BERT Mode
- CDR Mode
- Clock Synthesizer Mode



Depending on the mode enabled, various control and status indicators are available. BERT log files are generated and can be read from the PC for further use.

An API interface allows the pB10A to be integrated and controlled into an existing test setup using Microsoft Excel or LabView software environments.

Please contact support@pocketbert.com for any technical and commercial questions.

日本販売代理店
サンインスツルメント 株式会社
営業部
☎ 03-5436-9361 Fax : 03-5436-9364
✉ sun@sun-ins.com