40Gbps Parallel Active Optical Cable (AOC)

Preliminary Datasheet

Features

- 4 independent full-duplex channels
- Up to 12.5Gbps data rate per channel
- QSFP MSA compliant
- Up to 100m transmission
- Operating case temperature: 0~70C
- Single 3.3V power supply
- Typical 0.8W operation power each terminal
- RoHS compliant

- Infiniband SDR/DDR/QDR
- 2/4/8 G Fiber Channel

1. General Description

This product is a high data rate parallel active optical cable (AOC), to overcome the bandwidth limitation of traditional copper cable. The AOC offers 4 independent data transmission channels and 4 data receiving channels via the multimode ribbon fibers, each capable of 10Gbps operation. Consequently, an aggregate data rate of 40Gbps over 100 meters transmission can be achieved by this product, to support the ultra-fast computing data exchange.

This product is designed with form factor, optical/electrical connection according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

2. Functional Description

This product converts the parallel electrical input signals into parallel optical signals (light), by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The light propagates through the ribbon fiber individually, and be captured by the photo diode array. The optical signals are converted into parallel electrical signals and outputted. Consequently, each terminal of the cable has 8 ports, 4 for data transmission and 4 for data receiving, to provide totally 40Gbs data exchange. Figure 1 shows the functional block diagram of the parallel AOC.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP memory map.

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. When "Low", it indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

3. AOC Block Diagram

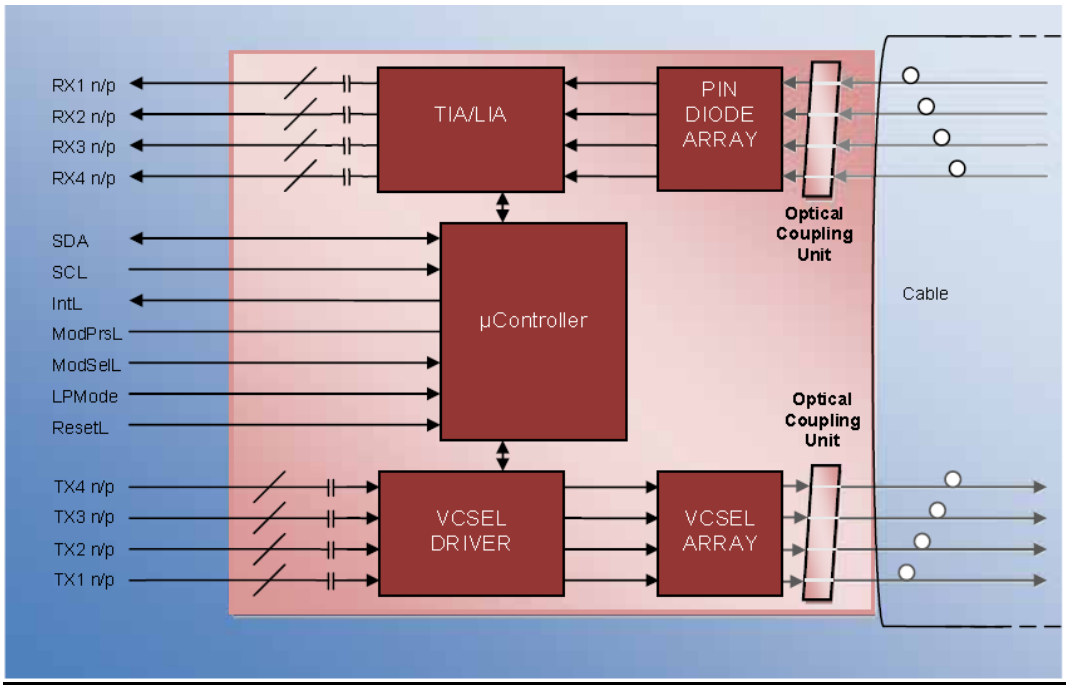


Figure 1: Block Diagram of one of the QSFP End Module

4. Pin Assignment and Pin Description

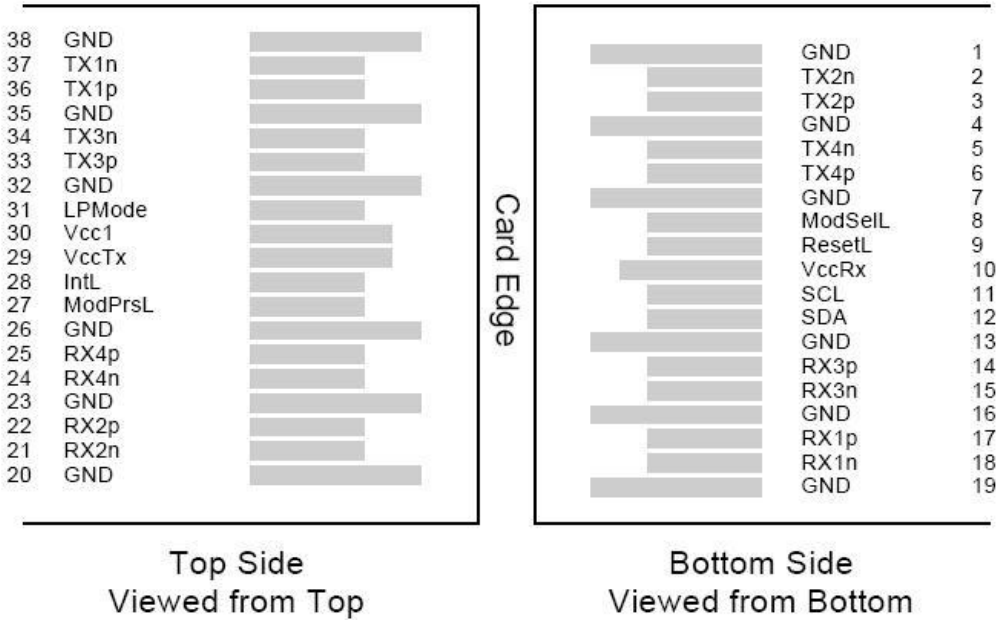


Figure 2: MSA compliant Connector

5. Pin Definitions.

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	

14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

6. General Information

Parameter	Typical Value	Unit	Notes
Number of Lanes	4 Tx & 4 Rx		
Date Rate, each Lane	10.5	Gb/s	
Maximum Aggregate Data Rate	42.0	Gb/s	
Bit Error Ratio	$<10^{-12}$		
Interface	Serial, I2C-based		defined by the QSFP MSA
Power Consumption, each terminal	0.8	W	
Operation Temperature	0-70	degC	

7. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH	0	85	%	
Operating Case Temperature	Topc	0	70	degC	
Supply Voltage	VCC		3.6	V	

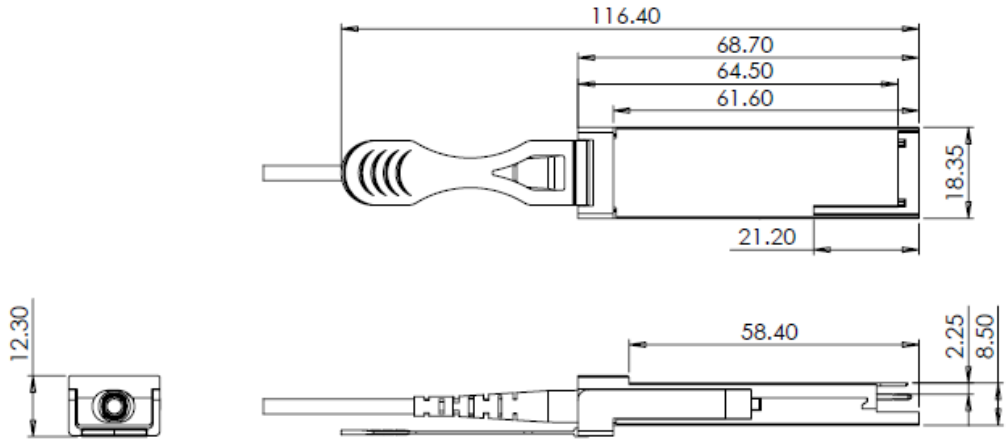
8. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating temperature and supply voltage unless otherwise specified.

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Supply Voltage	Vccl, VccTx, VccRx	3.1	3.3	3.4	V	
Supply Current	Icc		280	350	mA	
Transmit Turn-On Time				2	s	

Tx (each Lane)						
Reference Differential Input Impedance	Z_d		100		Ω	
Input AC Common Mode Voltage				25	mV (RMS)	
Differential Input S-parameter	SDD11	< -12 + 2 × SQRT(f), with f in GHz.			dB	0.01-4.1GHz
		< -6.3 + 13 × log10(f/5.5), with f in GHz			dB	4.1-11.1GHz
Reflected Differential to Common Mode Conversion	SCD11			-10	dB	0.01-11.1GHz
Total Jitter				0.40	UI	
Deterministic Jitter				0.15	UI	
Rx (each Lane)						
Reference Differential Input Impedance	Z_d		100		Ω	
Output AC Common Mode Voltage				15	mV (RMS)	
Differential Output S-parameter	SDD22	< -12 + 2 × SQRT(f), with f in GHz			dB	0.01-4.1GHz
		< -6.3 + 13 × log10(f/5.5), with f in GHz			dB	4.1-11.1GHz
Common Mode Output Reflection Coefficient	SCC22	< -7 + 1.6 × f, with f in GHz.			dB	0.01-2.5GHz
				-3	dB	2.5-11.1GHz
Total Jitter				0.38	UI	In case the Tx jitters are meet
Deterministic Jitter				0.64	UI	

9. Mechanical Dimensions



10. ESD

This transceiver is specified as ESD threshold 2kV for all electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

11. Ordering Information

When ordering QSFP AOC, a 10-character suffix is used to fully specify the part number. The part number's suffix has 3 separate elements, as explained below.

TF	-	X	X	XXX	-	X	XX
AOC Product		Product Form Factor Q: QSFP	Bit-rate Q: 40Gb/s	Range 100=100m; 005=5m;		Temperature N: 0 to 70C	Customized Code 00: Standard

Example

A part number of "TF–QQ100-N00" represents 100m QSFP AOC, "TF–QQ050-N00" represents 50m QSFP AOC

USA	China
InnoLight Technology Corp. Tel: (408) 861-3560 Fax: (408) 777-8091 Email: omok@innolight.com Address: Acorn Campus, 3 Results Way, Cupertino, CA 95014	InnoLight Technology (Suzhou) Ltd. Tel: (0512) 8666-9288 Fax: (0512) 8666-9299 Email: jyang@innolight.com Address: 328 Xinghu Street,12-A3, Suzhou Industrial Park, Suzhou, Jiangsu Province, 215123,China

Contact Information