40Gb/s QSFP Passive Copper Cable

TC-QQCOx-V00

Features

- Hot pluggable QSFP passive cable assembly
- 4 independent duplex channels operating at 10Gbps, also support for 2.5Gbps, 5Gbps data rates
- Proven link length up to 5 meters over 8 pairs 26-30AWG cables
- Compliant QSFP MSA specifications
- Operating case temperature: -40 to 85°C
- All-metal housing for superior EMI performance, low Near-End Crosstalk(NEXT)
- Precision process control for minimization of pair-to-pair skew
- Pull-to-release latch for easy installation
- RoHS compliant

Applications

- InfiniBand-SDR, DDR, QDR
- Computer cluster cross-connect
- Switches, Routers, and HBA's
- Enterprise Data Center
- High Performance Computing(HPC) & Storage

1. GENERAL DESCRIPTION

The InnoLight QSFP passive cable assembly is specifically designed to allow the end-user an high speed cable connection solution between ports based on QSFP connectivity, respectively. The cable is plug-and-play into these powered ports and provides the customer with all the advantages of a cost effective & easy to handle high speed connection. The transmitter side accepts electrical input signals which are voltage compatible with both Low Voltage Positive Emitter Coupled Logic (LVPECL) and Current Mode Logic (CML) levels. All data signals are differential and support a data rate up to 10Gbps per channel. All transmitter signals and receiver signals are AC coupled internally on both modules ends.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. The module offers 4 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA and ModPrsL.

Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP module must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP memory map.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state.

2. QSFP Copper Design Structure

InnoLight QSFP passive copper cable assembly includes one pair (A-B) QSFP modules connected by 26AWG cable which have 8 pair differential cables inside, the available cable lengths are from 1 to 5 meters, there are five different types.

Part Number	Diameter (mm)	Length (m)
TC-QQCOO-V00	7.11	1
TC-QQCOH-V00	7.11	3
TC-QQCOV-V00	7.11	5

3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	125	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Operating Case Temperature	Topc	-40	85	degC	1
Supply Voltage	VCC3	-0.3	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.3	VCC3 + 0.2	V	

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not applied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Topc	-40	85	degC
Relative Humidity (non-condensing)	Rhop	-	85	%
Power Supply Voltage	VCC3	3.135	3.465	V
Power Supply Current	ICC3	-	30	mA
Total Power Consumption	Pd	-	0.1	W

5. DC Low Speed Control and Alarm Signals Electrical Interface

Parameter	Conditions	Symbol	Min	Typ.	Max	Units
Supply Current	@ VCCT	IVCC		10	30	mA
Power Consumption				0.03	0.1	W
ModPrsl	Host Vcc Range 2V – 3.47V	VOL	0		0.4	V
		VOH	Host_Vcc – 0.5		Host_Vcc + 0.3	
ModeSelL	Low Voltage TTL	VIL	0.3		0.8	
		VIH	2		VccT + 0.3	
SCL, SDA	Host Vcc Range 3.14V – 3.47V	VIL	0.3		VccT*0 .3	
		VIH	VccT*0 .7		VccT + 0.5	
		VOL	0		0.4	
		VOH	Host_Vcc – 0.5		Host_Vcc + 0.3	

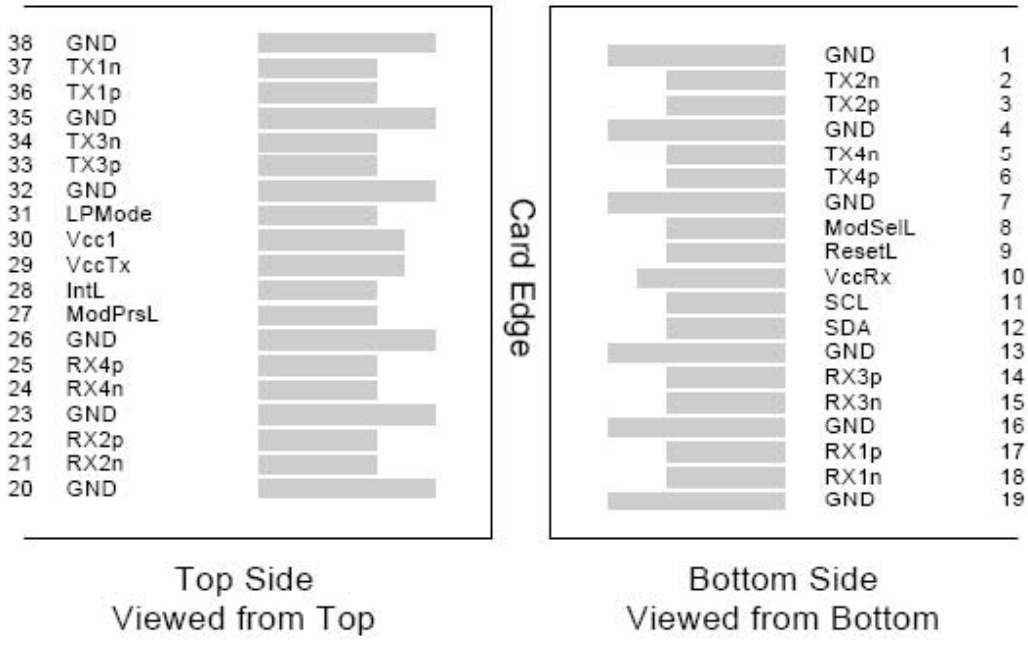
6. Module Transmitter Single Channel Input Characteristics

Parameter	Conditions	Symbol	Min	Typ.	Max	Units
Nominal Data Rate		DR	2.49	10	11.3	Gbps
Reference Differential Input Impedance		Zd	80	100	120	Ω
Input AC Common Mode Input Voltage			0		20	mV (RMS)
Differential Input Voltage Swing		VID	100		1200	mV

7. Module Receiver Single Channel Output Characteristics

Parameter	Conditions	Symbol	Min	Typ.	Max	Units
Nominal Data Rate		DR	2.49	10	11.3	Gbps
Reference Differential Output Impedance		Zd	80	100	120	Ω
Differential Output Amplitude	RLoad = 100Ohm, Differential	VOSPP	370		800	mV
Output Rise and Fall time	20% to 80%	tRH, tFH	30			ps
Receiver Output Deterministic Jitter		DJ			10	ps
Receiver Output Total Jitter	@10Gbps (BER 10^{-12})	TJ			25	ps

8. Pin Assignments and Descriptions

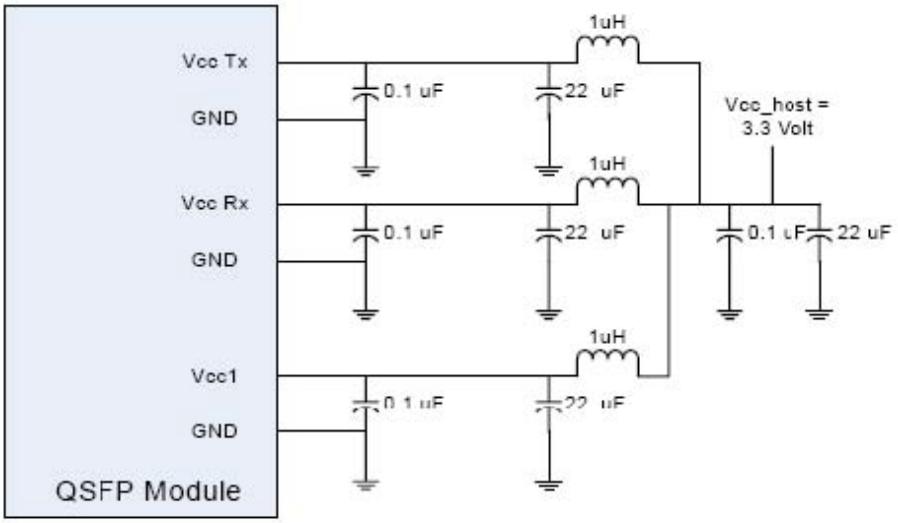


PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Not used	
10		Vcc Rx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CMLO	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CMLO	Rx1p	Receiver Non-Inverted Data Output	
18	CMLO	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CMLO	Rx2n	Receiver Inverted Data Output	
22	CMLO	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CMLO	Rx4n	Receiver Inverted Data Output	1
25	CMLO	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTLO	ModPrsL	Module Present	
28	LVTTLO	IntL	Not used	
29		Vcc Tx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTLI	LPMode	Not used	
32		GND	Ground	1
33	CMLI	Tx3p	Transmitter Non-Inverted Data Input	
34	CMLI	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CMLI	Tx1p	Transmitter Non-Inverted Data Input	
37	CMLI	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane.

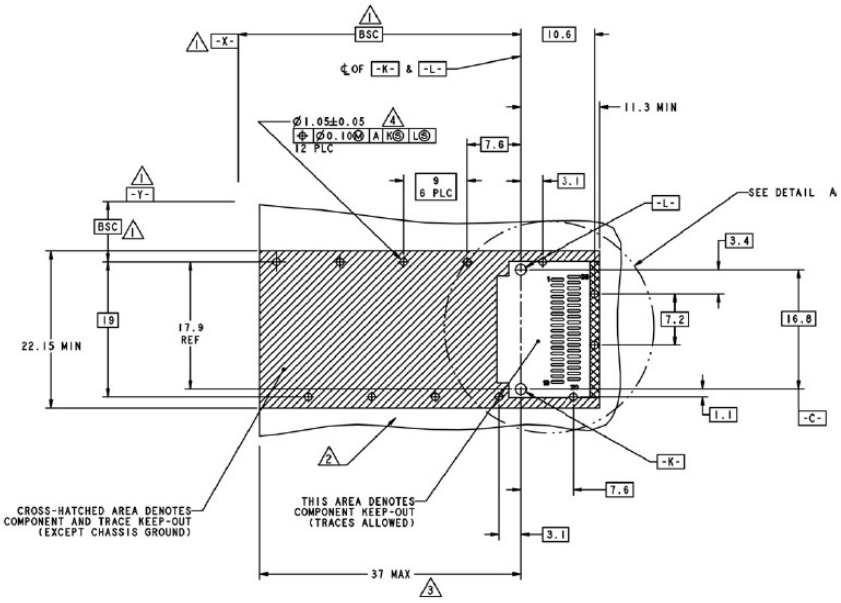
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

9. Recommended power supply filtering Example of QSFP Host board schematics.

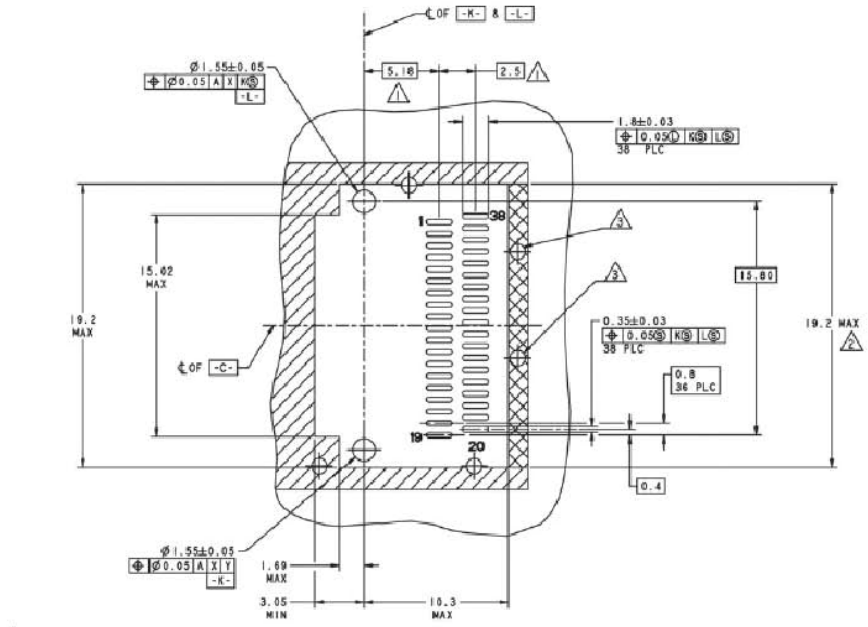


10. Recommended PCB layout

A typical host board mechanical layout for attaching the QSFP transceiver is presented below. The recommended host electrical connector should be a 38-pin IPASS right angle connector assembly (example: Tyco PN: 1761987-9) and the cage assembly should be QSFP single cage (example: Tyco PN: 1888617-1).

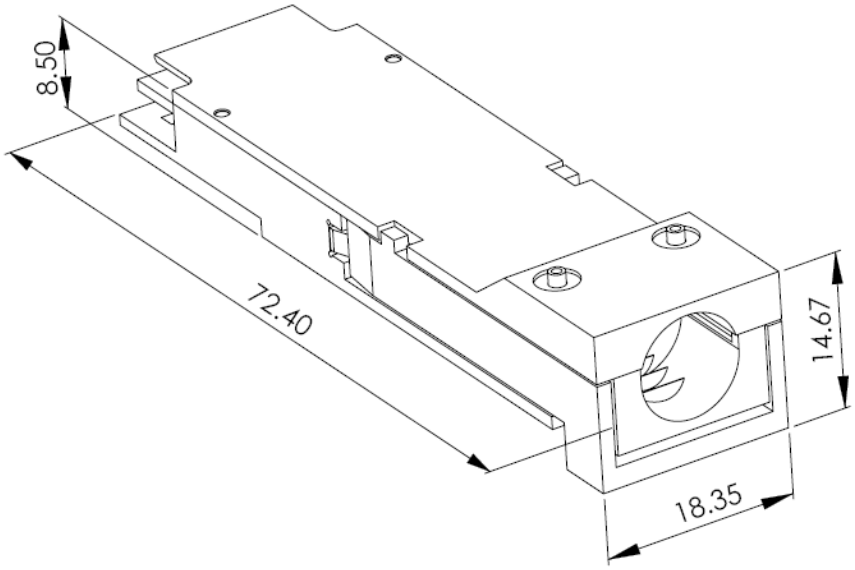


1 DATUM -X- AND -Y- ESTABLISHED BY CUSTOMER'S FIDUCIAL
2 DATUM -A- IS TOP SURFACE OF HOST BOARD.
3 LOCATION OF EDGE OF PCB IS APPLICATION SPECIFIC.
4 FINISHED HOLE SIZE.



1 CENTERLINE OF PAD.
2 SURFACE TRACES PERMITTED WITHIN THIS LENGTH.
3 INDICATED HOLES ARE OPTIONAL.

QSFP Copper Module Outline for System Design



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